CLAIMS

What is claimed is:

1. A method for 8b/10b encoding, the method comprising:

receiving an input running disparity;

receiving an 8-bit input that includes a 5-bit input portion and a 3-bit input portion;

determining, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, the input running disparity, and the 5-bit input portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 3-bit input portion;

determining a 6-bit output based on the 6-bit running disparity and the 5-bit input portion; and

determining a 4-bit output based on the 4-bit running disparity and the 3-bit input portion, wherein the 6-bit output and the 4-bit output provide a 10-bit encoded output.

2. The method of claim 1, wherein the determining the 6-bit running disparity further comprises:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 5-bit input portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 5-bit input portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 5-bit input portion is within a second set of values.

3. The method of claim 1, wherein the determining the 4-bit running disparity further comprises:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

4. The method of claim 1, wherein the determining the 6-bit output further comprises:

establishing the 6-bit output from the 5-bit input portion when the 5-bit input portion is of a value within a first set of values;

equating a first 6-bit value as the 6-bit output when the 6-bit running disparity is in a first state and the 5-bit input portion is of a value within a second set of values; and

equating a second 6-bit value as the 6-bit output when the 6-bit running disparity is in a second state and the 5-bit input portion is of a value within the second set of values.

5. The method of claim 1, wherein the determining the 4-bit output further comprises:

establishing the 4-bit output from the 3-bit input portion when the 3-bit input portion is of a value within a first set of values;

equating a first 4-bit value as the 4-bit output when the 4-bit running disparity is in a first state and the 3-bit input portion is of a value within a second set of values; and

equating a second 4-bit value as the 4-bit output when the 4-bit running disparity is in a second state and the 3-bit input portion is of a value within the second set of values.

6. A method for parallel 8b/10b encoding, the method comprising:

receiving an N-by-8-bit input;

performing, in parallel, 8b/10b encoding of N 8-bit input values of the N-by-8-bit input based on a plurality of running disparities for the N-by-8-bit input, wherein each of the N 8-bit input values includes a 5-bit input portion and a 3-bit input portion;

performing, in series, a running disparity calculation for each of the N 8-bit input values to produce the plurality of running disparities for the N-by-8-bit input, wherein the performing the running disparity calculation for one of the plurality of running disparities includes:

determining, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, an input running disparity, and the 5-bit input portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 3-bit input portion.

7. The method of claim 6, wherein the performing the 8b/10b encoding further comprises, for each of the N 8-bit input values:

determining a 6-bit output based on the 6-bit running disparity and the 5-bit input portion; and

determining a 4-bit output based on the 4-bit running disparity and the 3-bit input portion, wherein the 6-bit output and the 4-bit output provide a 10-bit encoded output.

8. The method of claim 7, wherein the determining the 6-bit output further comprises:

establishing the 6-bit output from the 5-bit input portion when the 5-bit input portion is of a value within a first set of values;

equating a first 6-bit value as the 6-bit output when the 6-bit running disparity is in a first state and the 5-bit input portion is of a value within a second set of values; and

equating a second 6-bit value as the 6-bit output when the 6-bit running disparity is in a second state and the 5-bit input portion is of a value within the second set of values.

9. The method of claim 7, wherein the determining the 4-bit output further comprises:

establishing the 4-bit output from the 3-bit input portion when the 3-bit input portion is of a value within a first set of values;

equating a first 4-bit value as the 4-bit output when the 4-bit running disparity is in a first state and the 3-bit input portion is of a value within a second set of values; and

equating a second 4-bit value as the 4-bit output when the 4-bit running disparity is in a second state and the 3-bit input portion is of a value within the second set of values.

10. The method of claim 6, wherein the determining the 6-bit running disparity further comprises:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 5-bit input portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 5-bit input portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 5-bit input portion is within a second set of values.

11. The method of claim 6, wherein the determining the 4-bit running disparity further comprises:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

12. A multi-gigabit transceiver comprising:

a transmitting section that includes a transmitter physical media attachment module and a transmitter physical coding sub-layer module, wherein the transmitter physical coding sub-layer module includes an 8b/10b encoding module that is operably coupled to:

receive an input running disparity;

receive an 8-bit input that includes a 5-bit input portion and a 3-bit input portion;

determine, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, the input running disparity, and the 5-bit input portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected

running disparity, the input running disparity, and the 3-bit input portion;

determine a 6-bit output based on the 6-bit running disparity and the 5-bit input portion; and

determine a 4-bit output based on the 4-bit running disparity and the 3-bit input portion, wherein the 6-bit output and the 4-bit output provide a 10-bit encoded output; and

a receiving section that includes a receiver physical media attachment module and a receiver physical coding sub-layer module, wherein the receiver physical coding sub-layer module includes an 8b/10b decoding module.

13. The multi-gigabit transceiver of claim 12, wherein the 8b/10b encoding module further functions to determine the 6-bit running disparity by:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 5-bit input portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 5-bit input portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 5-bit input portion is within a second set of values.

14. The multi-gigabit transceiver of claim 12, wherein the 8b/10b encoding module further functions to determine the 4-bit running disparity by:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

15. The multi-gigabit transceiver of claim 12, wherein the 8b/10b encoding module further functions to determine the 6-bit output by:

establishing the 6-bit output from the 5-bit input portion when the 5-bit input portion is of a value within a first set of values;

equating a first 6-bit value as the 6-bit output when the 6-bit running disparity is in a first state and the 5-bit input portion is of a value within a second set of values; and

equating a second 6-bit value as the 6-bit output when the 6-bit running disparity is in a second state and the 5-bit input portion is of a value within the second set of values.

16. The multi-gigabit transceiver of claim 12, wherein the 8b/10b encoding module further functions to determine the 4-bit output by:

establishing the 4-bit output from the 3-bit input portion when the 3-bit input portion is of a value within a first set of values;

equating a first 4-bit value as the 4-bit output when the 4-bit running disparity is in a first state and the 3-bit input portion is of a value within a second set of values; and

equating a second 4-bit value as the 4-bit output when the 4-bit running disparity is in a second state and the 3-bit input portion is of a value in the second set of values.

17. A multi-gigabit transceiver comprising:

a transmitting section that includes a transmitter physical media attachment module and a transmitter physical coding sub-layer module, wherein the transmitter physical coding

sub-layer module includes a parallel 8b/10b encoding module that is operably coupled to:

receive an N-by-8-bit input;

perform, in parallel, 8b/10b encoding of N 8-bit input values of the N-by-8-bit input based on a plurality of running disparities for the N-by-8-bit input, wherein each of the N 8-bit input values includes a 5-bit input portion and a 3-bit input portion;

perform, in series, a running disparity calculation for each of the N 8-bit input values to produce the plurality of running disparities for the N-by-8-bit input, wherein the performing the running disparity calculation for one of the plurality of running disparities includes:

determine, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, an input running disparity, and the 5-bit input portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 3-bit input portion; and

a receiving section that includes a receiver physical media attachment module and a receiver physical coding sub-layer module, wherein the receiver physical coding sub-layer module includes an 8b/10b decoding module.

18. The multi-gigabit transceiver of claim 17, wherein the 8b/10b encoding module further functions to perform the 8b/10b encoding by, for each of the N 8-bit input values:

determining a 6-bit output based on the 6-bit running disparity and the 5-bit input portion; and

determining a 4-bit output based on the 4-bit running disparity and the 3-bit input portion, wherein the 6-bit output and the 4-bit output provide a 10-bit encoded output.

19. The multi-gigabit transceiver of claim 18, wherein the 8b/10b encoding module further functions to determine the 6-bit output by:

establishing the 6-bit output from the 5-bit input portion when the 5-bit input portion is of a value within a first set of values;

equating a first 6-bit value as the 6-bit output when the 6-bit running disparity is in a first state and the 5-bit input portion is of a value within a second set of values; and

equating a second 6-bit value as the 6-bit output when the 6-bit running disparity is in a second state and the 5-bit input portion is of a value within the second set of values.

20. The multi-gigabit transceiver of claim 18, wherein the 8b/10b encoding module further functions to determine the 4-bit output by:

establishing the 4-bit output from the 3-bit input portion when the 3-bit input portion is of a value within a first set of values;

equating a first 4-bit value as the 4-bit output when the 4-bit running disparity is in a first state and the 3-bit input portion is of a value within a second set of values; and

equating a second 4-bit value as the 4-bit output when the 4-bit running disparity is in a second state and the 3-bit input portion is of a value within the second set of values.

21. The multi-gigabit transceiver of claim 17, wherein the 8b/10b encoding module further functions to determine the 6-bit running disparity by:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 5-bit input portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 5-bit input portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 5-bit input portion is within a second set of values.

22. The multi-gigabit transceiver of claim 17, wherein the 8b/10b encoding module further functions to determine the 4-bit running disparity by:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

23. A method for decoding an 8b/10b encoded data word, the method comprising:

receiving a 10-bit encoded data word having a 6-bit portion and a 4-bit portion;

receiving a running disparity;

determining, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, the running disparity, and the 6-bit portion, and

wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 4-bit portion;

determining a 5-bit decoded value based on the 6-bit running disparity and the 6-bit portion; and

determining a 3-bit decoded value based on the 4-bit running disparity and the 4-bit portion, wherein the 5-bit decoded value and the 3-bit decoded value provide an 8-bit decoded value.

24. The method of claim 23, wherein the determining the 6-bit running disparity further comprises:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 6-bit portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 6-bit portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 6-bit portion is within a second set of values.

25. The method of claim 23, wherein the determining the 4-bit running disparity further comprises:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

26. The method of claim 23, wherein the determining the 5-bit decoded value further comprises:

establishing the 5-bit decoded value from the 6-bit portion when the 6-bit portion is of a value within a first set of values;

equating a first 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a first state and the 6-bit portion is of a value within a second set of values; and

equating a second 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a second state and the 6-bit portion is of a value within the second set of values.

27. The method of claim 23, wherein the determining the 3-bit decoded further comprises:

establishing the 3-bit decoded value from the 4-bit portion when the 4-bit portion is of a value within a first set of values;

equating a first 3-bit value as the 3-bit decoded value when the 4-bit running disparity is in a first state and the 4-bit portion is of a value within a second set of values; and

equating a second 3-bit value as the 3-bit decoded when the 4-bit running disparity is in a second state and the 4-bit portion is of a value within the second set of values.

28. A method for parallel 8b/10b decoding, the method comprising:

receiving an encoded N-by-10-bit input;

performing, in parallel, 8b/10b decoding of N 10-bit input values of the encoded N-by-10-bit input based on a plurality of running disparities for the encoded N-by-10-bit input, wherein each of the N 10-bit input values includes a 6-bit portion and a 4-bit portion;

performing, in series, a running disparity calculation for each of the N 10-bit input values to produce the plurality of running disparities for the encoded N-by-10-bit input, wherein the performing the running disparity calculation for one of the plurality of running disparities includes:

determining, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, an input running disparity, and the 6-bit portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 4-bit portion.

29. The method of claim 28, wherein the performing the 8b/10b decoding further comprises, for each of the N 10-bit input values:

determining a 5-bit decoded value based on the 6-bit running disparity and the 6-bit portion; and

determining a 3-bit decoded value based on the 4-bit running disparity and the 4-bit portion, wherein the 5-bit decoded value and the 3-bit decoded value provide an 8-bit decoded output.

30. The method of claim 29, wherein the determining the 5-bit decoded value further comprises:

establishing the 5-bit decoded value from the 6-bit portion when the 6-bit portion is of a value within a first set of values;

equating a first 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a first state and the 6-bit portion is of a value within a second set of values; and

equating a second 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a second state and the 6-bit portion is of a value within the second set of values.

31. The method of claim 29, wherein the determining the 3-bit decoded value further comprises:

establishing the 3-bit decoded value from the 4-bit portion when the 4-bit portion is of a value within a first set of values;

equating a first 3-bit value as the 3-bit decoded value when the 4-bit running disparity is in a first state and the 4-bit portion is of a value within a second set of values; and

equating a second 3-bit value as the 3-bit decoded value when the 4-bit running disparity is in a second state and the 4-bit portion is of a value within the second set of values.

32. The method of claim 28, wherein the determining the 6-bit running disparity further comprises:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input

running disparity is in a first state and the 6-bit portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 6-bit portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 6-bit portion is within a second set of values.

33. The method of claim 28, wherein the determining the 4-bit running disparity further comprises:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

34. A multi-gigabit transceiver comprises:

a transmitting section that includes a transmitter physical media attachment module and a transmitter physical coding sub-layer module, wherein the transmitter physical coding sub-layer module includes a parallel 8b/10b encoding module; and

a receiving section that includes a receiver physical media attachment module and a receiver physical coding sub-layer module, wherein the receiver physical coding sub-layer module includes an 8b/10b decoding module that is operably coupled to:

receive a 10-bit encoded data word having a 6-bit portion and a 4-bit portion;

receive a running disparity;

determining, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, the running disparity, and the 6-bit portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running

disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 4-bit portion;

determine a 5-bit decoded value based on the 6-bit running disparity and the 6-bit portion; and

determine a 3-bit decoded value based on the 4-bit running disparity and the 4-bit portion, wherein the 5-bit decoded value and the 3-bit decoded value provide an 8-bit decoded value.

35. The multi-gigabit transceiver of claim 34, wherein the 8b/10b decoding module further functions to determine the 6-bit running disparity by:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 6-bit portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 6-bit portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 6-bit portion is within a second set of values.

36. The multi-gigabit transceiver of claim 34, wherein the 8b/10b decoding module further functions to determine the 4-bit running disparity by:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running

disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

37. The multi-gigabit transceiver of claim 34, wherein the 8b/10b decoding module further functions to determining the 5-bit decoded value by:

establishing the 5-bit decoded value from the 6-bit portion when the 6-bit portion is of a value within a first set of values;

equating a first 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a first state and the

6-bit portion is of a value within a second set of values; and

equating a second 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a second state and the 6-bit portion is of a value within the second set of values.

38. The multi-gigabit transceiver of claim 34, wherein the 8b/10b decoding module further functions to determine the 3-bit decoded by:

establishing the 3-bit decoded value from the 4-bit portion when the 4-bit portion is of a value within a first set of values;

equating a first 3-bit value as the 3-bit decoded value when the 4-bit running disparity is in a first state and the 4-bit portion is of a value within a second set of values; and

equating a second 3-bit value as the 3-bit decoded when the 4-bit running disparity is in a second state and the 4-bit portion is of a value within the second set of values.

39. A multi-gigabit transceiver comprises:

a transmitting section that includes a transmitter physical media attachment module and a transmitter physical coding sub-layer module, wherein the transmitter physical coding sub-layer module includes a parallel 8b/10b encoding module; and

a receiving section that includes a receiver physical media attachment module and a receiver physical coding sub-layer module, wherein the receiver physical coding sub-layer

module includes an 8b/10b decoding module that is operably coupled to:

receive an encoded N-by-10-bit input;

perform, in parallel, 8b/10b decoding of N 10-bit input values of the encoded N-by-10-bit input based on a plurality of running disparities for the encoded N-by-10-bit input, wherein each of the N 10-bit input values includes a 6-bit portion and a 4-bit portion;

perform, in series, a running disparity calculation for each of the N 10-bit input values to produce the plurality of running disparities for the encoded N-by-10-bit input, wherein the performing the running disparity calculation for one of the plurality of running disparities includes:

determining, in parallel, a 6-bit running disparity and a 4-bit running disparity, wherein the 6-bit running disparity is based on a first possible 6-bit expected running disparity, a second possible 6-bit expected running disparity, an input running disparity, and the 6-bit portion, and wherein the 4-bit running disparity is based on the first possible 6-bit expected running disparity, the second possible 6-bit expected running disparity, a first possible 4-bit expected running disparity, a second possible 4-bit expected running disparity, the input running disparity, and the 4-bit portion.

40. The multi-gigabit transceiver of claim 39, wherein the 8b/10b decoding module further functions to performing the 8b/10b decoding by, for each of the N 10-bit input values:

determining a 5-bit decoded value based on the 6-bit running disparity and the 6-bit portion; and

determining a 3-bit decoded value based on the 4-bit running disparity and the 4-bit portion, wherein the 5-bit decoded value and the 3-bit decoded value provide an 8-bit decoded output.

41. The multi-gigabit transceiver of claim 40, wherein the 8b/10b decoding module further functions to determine the 5-bit decoded value by:

establishing the 5-bit decoded value from the 6-bit portion when the 6-bit portion is of a value within a first set of values;

equating a first 5-bit value as the 5-bit decoded value when the 6-bit running disparity is in a first state and the 6-bit portion is of a value within a second set of values; and

equating a second 5-bit value as the 5-bit decoded value when the 6-bit running disparity is within a second state and the 6-bit portion is of a value in the second set of values.

42. The multi-gigabit transceiver of claim 40, wherein the 8b/10b decoding module further functions to determine the 3-bit decoded value further comprises:

establishing the 3-bit decoded value from the 4-bit portion when the 4-bit portion is of a value within a first set of values;

equating a first 3-bit value as the 3-bit decoded value when the 4-bit running disparity is in a first state and the

4-bit portion is of a value within a second set of values; and

equating a second 3-bit value as the 3-bit decoded value when the 4-bit running disparity is in a second state and the 4-bit portion is of a value within the second set of values.

43. The multi-gigabit transceiver of claim 39, wherein the 8b/10b decoding module further functions to determine the 6-bit running disparity by:

selecting the first possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a first state and the 6-bit portion is within a first set of values;

selecting the second possible 6-bit expected running disparity as the 6-bit running disparity when the input running disparity is in a second state and the 6-bit portion is within the first set of values; and

setting the 6-bit running disparity to substantially equal the input running disparity when the 6-bit portion is within a second set of values.

44. The multi-gigabit transceiver of claim 39, wherein the 8b/10b decoding module further functions to determine the 4-bit running disparity by:

selecting the first possible 4-bit expected running disparity as a first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a first state;

selecting the second possible 4-bit expected running disparity as the first intermediate 4-bit expected running disparity when the first possible 6-bit expected running disparity is in a second state;

selecting the first possible 4-bit expected running disparity as a second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a third state;

selecting the second possible 4-bit expected running disparity as the second intermediate 4-bit expected running disparity when the second possible 6-bit expected running disparity is in a fourth state;

selecting the first intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a fifth state; and

selecting the second intermediate 4-bit expected running disparity as the 4-bit running disparity when the input running disparity is in a sixth state.

45. A method for encoding/decoding, the method comprising:

receiving an input running disparity;

receiving an (M+N)-bit input that includes a M-bit input portion and a N-bit input portion, wherein M and N are integers;

determining, in parallel, an X-bit running disparity and a Y-bit running disparity, wherein the X-bit running disparity is based on a first possible X-bit expected running disparity, a second possible X-bit expected running disparity, the input running disparity, and the M-bit input

portion, and wherein the Y-bit running disparity is based on the first possible X-bit expected running disparity, the second possible X-bit expected running disparity, a first possible Y-bit expected running disparity, a second possible Y-bit expected running disparity, the input running disparity, and the N-bit input portion;

determining a X-bit output based on the X-bit running disparity and the M-bit input portion; and

determining a Y-bit output based on the Y-bit running disparity and the N-bit input portion, wherein the X-bit output and the Y-bit output provide a (X+Y)-bit encoded output;

wherein X is an integer greater than M, and Y is an integer greater than N.